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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Paul Shirley et al.	§	Group Art Unit:	2823
Serial No.: 10/765,481	§	Examiner:	Toledo, Fernando L.
Filed: January 27, 2004	§		
For: METHOD AND APPARARTUS FOR A TWO-STEP RESIST SOFT BAKE TO PREVENT ILD OUTGASSING DURING SEMICONDUCTOR PROCESSING	§	Atty. Docket:	MICS:0117/FLE/FAR 02-1051

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37 C.F.R. 1.8

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November 6, 2006 — Michael G. Fletcher
Date

APPEAL BRIEF PURSUANT TO 37 C.F.R. §§ 41.31 AND 41.37

This Appeal Brief is being filed in furtherance to the Notice of Appeal mailed on September 1, 2006, and received by the Patent Office on September 6, 2006.

The Commissioner is authorized to charge the requisite fee of $500.00 for the Appeal Brief, and any additional fees which may be required, to the credit card listed on the attached PTO-2038. However, if the PTO-2038 is missing, if the amount listed thereon is insufficient, or if the amount is unable to be charged to the credit card for any other reason, the Commissioner is authorized to charge Deposit Account No. 06-1315; Order No. MICS:0117:FLE/FAR (02-1051).

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1. REAL PARTY IN INTEREST

The real party in interest is Micron Technology, Inc., the Assignee of the above-referenced application by virtue of the Assignment to Micron Technology, Inc. recorded at reel 014930, frame 0703, and dated January 27, 2004. Accordingly, Micron Technology, Inc., will be directly affected by the Board's decision in the pending appeal.

2. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any other appeals or interferences related to this Appeal. The undersigned is Appellants' legal representative in this Appeal.

3. STATUS OF CLAIMS

Claims 1-12 are currently pending, are currently under final rejection and, thus, are the subject of this Appeal.

4. STATUS OF AMENDMENTS

As the instant claims have not been amended at any time, there are no outstanding amendments to be considered by the Board.

5. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates generally to the fabrication of integrated circuits and, more particularly, to soft baking a semiconductor wafer so that photo resist layers are free of surface voids or craters. Application, page 2, lines 8-10. The present

application contains two independent claims, namely, claims 1 and 12, both of which are the subject of this Appeal. The subject matter of these two independent claims is summarized below. Further, the subject matter of dependent claims 9 and 10 are also summarized.

Independent Claims

Independent claim 1 recites a method of soft-baking a semiconductor wafer substrate, including: soft-baking a substrate (e.g., semiconductor wafer 10 having a substrate 12) coated with a resist (e.g., photoresist 18) at a first temperature (e.g., within a range of 30-75 °C) for a first predetermined period of time (e.g., within a range of 30-90 seconds); and then soft-baking the substrate coated with the resist at a second higher temperature (e.g., within a range of 90-150 °C) for a second predetermined period of time (e.g., within a range of 90-150 °C). *See, e.g.,* Application, page 7, lines 7-18; page 9, lines 12-21; page 10, lines 15-23; Figure 1.

Independent claim 12 recites a semiconductor wafer (e.g., wafer 10) having a resist layer (e.g., photo resist 18) without craters at the completion of a two-part soft bake of the semiconductor wafer. *See, e.g.,* page 7, line 7 – page 9, line 23; page 10, line 15 – page 11, line 21; Figure 1-3.

Dependent Claims 9 and 10

Claim 9 depends from the method of claim 1 and recites that the higher temperature is in the range of 100-130 °C. *See, e.g.,* page 11, lines 17-21. Claim 10 depends from claim 1 and recites that the second predetermined period of time is less than 90 seconds. *See, e.g., id.*

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

First Ground of Rejection for Review on Appeal:

Appellants respectfully urge the Board to review and reverse the Examiner's first ground of rejection in which the Examiner rejected claims 1-8, 11, and 12 under 35 U.S.C. § 102(b) as being anticipated by pages 429, 434-437, 452, and 453 of Wolf and Tauber (Silicon Processing for the VLSI Era Volume 1: Process Technology), hereinafter "Wolf."

Second Ground of Rejection for Review on Appeal:

Appellants respectfully urge the Board to review and reverse the Examiner's second ground of rejection in which the Examiner rejected dependent claims 9 and 10 under 35 U.S.C. 103(a) as being unpatentable over Wolf as applied to claims 1-7.

7. ARGUMENT

As discussed in detail below, the Examiner has improperly rejected the pending claims. Further, the Examiner has misapplied long-standing and binding legal precedents

and principles in rejecting the claims under Sections 102 and 103. Accordingly, Appellants respectfully request full and favorable consideration by the Board, as Appellants strongly believe that claims 1-12 are currently in condition for allowance.

A. **Ground of Rejection No. 1**

Claims 1-8, 11, and 12 were rejected under 35 U.S.C. 102(b) as being anticipated by Wolf. Claims 1 and 12 are independent. Appellants respectfully traverse this rejection.

Legal Precedent

Anticipation under Section 102 can be found only if a single reference shows exactly what is claimed. *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 227 U.S.P.Q. 773 (Fed. Cir. 1985). Every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). The prior art reference must show the *identical* invention "*in as complete detail as contained in the ... claim*" to support a *prima facie* case of anticipation. *Richardson v. Suzuki Motor Co.*, 9 U.S.P.Q. 2d 1913, 1920 (Fed. Cir. 1989) (emphasis added).

Further, during patent examination, the pending claims must be given an interpretation that is reasonable and consistent with the specification. *See In re Prater*, 415 F.2d 1393, 1404-05, 162 U.S.P.Q. 541, 550-51 (C.C.P.A. 1969); *see also* M.P.E.P. §§ 608.01(o) and 2111. Indeed, the specification is "the primary basis for construing the

claims." *See Phillips v. AWH Corp.*, No. 03-1269, -1286, at 13-16 (Fed. Cir. July 12, 2005) (citations omitted).

Independent Claims 1 and 12

Independent claims 1 and 12 recite a *two-step* soft-bake. The two-step soft-bake is employed to inhibit the formation of resist craters. *See, e.g.*, Application, page 9, line 12 – page 10, line 13. As disclosed, the initial first-step bake of the claimed soft-bake is performed at a temperature lower than traditional soft-bake temperatures. *Id.* In the subsequent second bake, the wafer is then subjected to a higher and more traditional soft-bake temperature. *Id.* As described in the specification, the inhibition of crater formation resulting from a two-step soft bake having a lower temperature in the first-bake step may be explained by one or more theories. *See, e.g.*, Application, page 9, line 12 – page 10, line 13; *see also Phillips*, at 16 (explaining that one should rely heavily on the written description for guidance as to the meaning of the claims).

One disclosed theory is that the initial lower-temperature bake drives the solvents (but not air) out of the resist, making the resist less fluid. *Id.* Thus, when the wafer is then baked at the subsequent regular and higher temperature, the resist has solidified enough so that the air can not pass through the resist which could cause resist craters. *Id.* A second theory is that the lower bake temperature allows the resist to remain fluid long enough so that the air, as it expands, can pass through the resist layer. *Id.* Then, the resist flows back to its original conformal shape. *Id.* During the subsequent higher temperature bake, the amount of air has been reduced to the point where the air does not

have the energy to pass through the hardening resist to cause resist craters. *Id.* Again, consequently, with the novel two-step soft-bake, as disclosed and claimed, the lower bake temperature of the first step inhibits formation of resist craters.

In contrast, the Wolf reference is absolutely devoid of a *two-step* soft-bake or any discussion of the formation of resist craters as related to the soft bake. Instead, Wolf teaches the typical *single-step* soft-bake and does not resolve resist crater formation. *See* pages 434-436; Fig. 14. To be sure, while Wolf also teaches a post-bake (which occurs after the soft-bake and after the resist has been exposed), Wolf does not even contemplate a *two-step* soft-bake. *See* Wolf, pages 434-437 and 452; Fig. 14 (disclosing only a single-step soft-bake); Application, page 4, lines 1-5; page 5; lines 1-2; page 8, lines 8-9 and 14-15; page 9, lines 15-19 (discussing an embodiment of a two-step soft bake). Therefore, the Wood reference cannot anticipate the present claims 1-12.

Previously, the Examiner incorrectly pointed to the Wolf post-bake as a second step of a soft bake. *See, e.g.*, Office Action Mailed November 9, 2005, page 2. However, in the "Response of Arguments" section of the Final Office Action, the Examiner changed his argument and focused instead on the infrared single-step soft-bake of Wolf. *See* Final Office Action, page 6 (citing Wolf, page 437 and Figure 12 (c)). Surprisingly, the Examiner argued that the time required for the wafer to reach the soft-bake temperature is somehow a separate soft-bake step, as claimed. *See id.* Indeed, the Examiner contended incorrectly that the ramp-up portion of the temperature curve of Fig. 12 (c) represents baking the Wolf wafer at a first temperature for a first predetermined

period of time. Yet, one of ordinary skill in the art would *not* view the warm-up of the wafer (or the cool-down of the wafer for that matter) as a separate and distinct soft-bake step conducted at *a* different temperature at a predetermined *period* of time, as claimed.

A wafer in any single-step soft bake, such as in the Wolf IR system, will generally warm to the desired bake temperature and then cool at the conclusion of the bake. Such behavior (a transition temperature region) could also be seen in the claimed two-step soft-bake, e.g., before and after each of the two baking steps. However, the two recited steps of claim 1 are not directed to the warm-up or other temperature transition of the wafer. Instead, claim 1 clearly recites a two-step soft bake, where the wafer is baked at "*a* first temperature for a first *predetermined period* of time" and at "*a* second *higher* temperature for a second *predetermined period* of time." Wolf fails to disclose these features.

Indeed, the Examiner cannot legitimately argue that the infinite number of instantaneous temperatures experienced by the Wolf wafer (during the temperature ramp of the Wolf wafer) can be a selected bake temperature for a predetermined period of time. Further, with regard to the specific numerical values (for temperature and time) mentioned by the Examiner, Appellants note that independent claims 1 and 12 do not recite numerical values or ranges. *See* Final Office Action, page 6. In view of the foregoing, Appellants respectfully assert that the Examiner has failed to establish a case of anticipation.

Claim Interpretation

In addition, in view of the *Phillips* case cited above, Appellants believe that the Examiner has improperly ignored the present specification in interpreting the claims. Indeed, the Examiner has imposed an awkward interpretation on the present claims in an effort to render the claims anticipated. For example, the Examiner failed to recognize the clear embodiments of the two-step soft-bake process described in the specification which support and provide context/interpretation of the present claims. Indeed, the specification clearly explains that a two-step soft bake is employed in lieu of the traditional single-step soft bake to avoid the formation of resist craters. *See, e.g.,* Application, page 9, lines 12-21. As discussed above, the initial step of the two-step soft bake, as disclosed and claimed in the present application, is performed at a lower temperature to inhibit formation of resist craters in the subsequent second step at the higher temperature of a soft bake. *See, e.g.,* Application, page 9, line 12 - page 10, line 13.

Again, it should be emphasized that each step of the two-step soft bake, as claimed, are performed at predetermined periods of time. Indeed, a period of time is required for the first step so that no resist craters are formed in the subsequent second step at the higher temperature bake. *See, e.g.,* Application, page 10, lines 1-13. In stark contrast, the Wolf reference discloses an infrared (IR) heating method (relied on by the Examiner) that is clearly a single-step soft bake with the Wolf wafer subjected to a constant amount of infrared radiation over a single period of time.

The present specification provides additional context for the claims such that a thermal unit (e.g., temperature chamber, hot plate, etc.) are cycled to the two different specified temperatures of the two-step soft bake. *See* Application, page 10, lines 15-22. Plainly, one could not appropriately equate the IR heating of Wolf with the two-step soft bake of the present claims. In sum, in view of the present specification and the plain language of the claims, Appellants believe the Examiner has imposed an incorrect interpretation on the claims in an effort to render the claims anticipated by an IR heating method at constant radiation.

Independent Claim 12

Independent claim 12 specifically recites "a semiconductor wafer comprising a resist layer without craters at the completion of a two-part soft bake." In contrast, while Wolf refers to the "pinhole concentration" in the resist layer, Wolf does *not* disclose a semiconductor wafer having a resist layer *without craters*. *See* pages 434-436; Fig. 14. The Examiner cited Fig. 14 of Wolf in support of his assertion that Wolf discloses a resist layer without craters. *See* Office Action, page 3. However, after careful review of the cited pages of the reference, Appellants emphasize that Wolf fails to even contemplate a semiconductor wafer having a resist layer *without craters*, much less disclose such a wafer. *See* Wolf, pages 429-437 and 452-453. Indeed, Wolf is absolutely devoid of a wafer having resist with no craters. Therefore, the Wolf reference cannot anticipate the claim 12 for this additional reason.

Request Withdrawal of Rejection

In view of these reasons, Appellants respectfully request that the Board direct the Examiner to withdraw the rejection of claims 1-8, 11, and 12 under 35 U.S.C. 102(b), and to allow the claims.

B. **Ground of Rejection No. 2**

Dependent claims 9 and 10 were rejected under 35 U.S.C. 103(a) as being unpatentable over Wolf as applied to claims 1-7 above. Appellants respectfully traverse this rejection.

Legal Precedent

The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (PTO Bd. App. 1979). To establish a *prima facie* case, the Examiner must not only show that a modified reference includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the reference. *See Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985). The Examiner must provide objective evidence, rather than subjective belief and unknown authority, of the requisite motivation or suggestion to combine or modify the cited references. *See In re Lee*, 61 U.S.P.Q.2d. 1430 (Fed. Cir. 2002). The Examiner cannot use hindsight reconstruction to pick and choose among isolated disclosures in the

prior art to deprecate the claimed invention. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988).

Claims 9 and 10

As discussed, Wolf fails to disclose the second soft-bake step recited in independent claim 1. Therefore, dependent claims 9 and 10 are patentable over Wolf by virtue of their dependency on an allowable base claim. Furthermore, as acknowledged by the Examiner, Wolf fails to disclose the specific temperature range and time period recited in claims 9 and 10, respectively. *See* Office Action, pages 4-5; Wolf, pages 429-437 and 452-453. Thus, dependent claims 9 and 10 are also patentable over Wolf because of the subject matter they separately recite.

Further, contrary to the Examiner's assertions, Appellants emphasize that the specific process conditions (i.e., temperature and time) associated with the second soft-bake step, as recited in dependent claims 9 and 10, are *not* obvious. *See* Office Action, pages 4-6. Indeed, without the benefit of the present application, one of ordinary skill in the art would not know to employ a two-step soft-bake, in general, much less a two-step soft-bake that utilizes the process conditions (of the second step) recited in claims 9 and 10. To be sure, Wolf teaches a much different bake timing. Again, the Wolf reference teaches the typical *single-step* soft-bake, does not resolve resist crater formation, and is oblivious to the concept of a *two-step* soft-bake.

Also, contrary to the Examiner's assertions on pages 4-6 of the Final Office Action, the unique results (e.g., no resist craters) associated with the new soft-bake (having a second baking step) with the claimed process conditions are discussed in the present specification. *See, e.g.*, Application, page 9, lines 12-21. Without a doubt, the claimed first-step at a lower temperature combined with the claimed second-step at a higher temperature are discussed in the specification as being important to the invention, i.e., in the reason for and result of inhibiting the formation of resist craters . *See, e.g.*, page 9, line 12 – page 10, line 13.

In view of these reasons, Appellants respectfully request that the Board direct the Examiner to withdraw the foregoing rejection of claims 9 and 10 under 35 U.S.C. § 103(a), and to allow the claims.

Conclusion

Appellants respectfully submit that all pending claims are in condition for allowance. However, if the Examiner or Board wishes to resolve any other issues by way of a telephone conference, the Examiner or Board is kindly invited to contact the undersigned attorney at the telephone number indicated below.

Respectfully submitted,

Date: November 6, 2006

Michael G. Fletcher
Reg. No. 32,777
FLETCHER YODER
P.O. Box 692289
Houston, TX 77269-2289
(281) 970-4545

8. APPENDIX OF CLAIMS ON APPEAL

Listing of Claims:

1. A method of soft-baking a semiconductor wafer substrate, comprising the acts of:

(a) soft-baking a substrate coated with a resist at a first temperature for a first predetermined period of time; and

(b) after act (a), soft-baking the substrate coated with the resist at a second higher temperature for a second predetermined period of time.

2. The method, as set forth in claim 1, wherein no resist craters are formed.

3. The method, as set forth in claim 1, wherein during the first predetermined period of time:

the resist hardens; and

the air trapped under the resist does not possess sufficient energy to expand through the resist.

4. The method, as set forth in claim 1, wherein during the first predetermined period of time:

the resist remains fluid;

air trapped under the resist expands through the resist to the surface; and

the resist flows back to its original conformal shape.

5. The method, as set forth in claim 1, wherein the semiconductor wafer is subjected to a temperature in the range of 30-90 °C during the first predetermined period of time.

6. The method, as set forth in claim 1, wherein the first predetermined period of time is less than 90 seconds.

7. The method, as set forth in claim 1, wherein the first predetermined period of time is more than 90 seconds.

8. The method, as set forth in claim 1, wherein the higher temperature is in the range of 90-150 °C.

9. The method, as set forth in claim 1, wherein the higher temperature is in the range of 100-130 °C.

10. The method, as set forth in claim 1, wherein the second predetermined period of time is less than 90 seconds.

11. The method, as set forth in claim 1, wherein the second predetermined period of time is more than 90 seconds.

12. A semiconductor wafer comprising a resist layer without craters at the completion of a two-part soft bake of the semiconductor wafer.

13. – 28. (Cancelled)

9. EVIDENCE APPENDIX

None.

10. RELATED PROCEEDINGS APPENDIX

None.